Scalable Coherent Multi-Channel SDR VORTARIAN 4R2T-10G

Features

- Four coherent RF receive channels
- Two RF transmit channels
- 16-bit ADCs operating at 500 MSPS
- 16-bit DACs operating at 1 GSPS
- Direct RF / IF sampling 20 MHz to 1.4 GHz
- Frequency coverage extendable up to 75 GHz using optional RF mezzanine front-ends
- Efinix Titanium FPGA with integrated Quad-Core RISC-V SoC
- Dual 10GBASE-SR SFP+ interfaces
- External reference clock input
- Multi-board synchronization capability under development
- Low-jitter clock generation and distribution
- On-board LPDDR4 memory

Applications

- Passive/MIMO radar and distributed RF sensing
- Direction finding (DF) and angle-of-arrival (AoA) measurements
- Beamforming and phased-array research
- Coherent multi-channel signal acquisition
- Spectrum monitoring and RF signal intelligence
- Software-defined radio (SDR) prototyping
- Wireless communications research and development
- Distributed SDR architectures and future synchronized multi-board operation
- Electronic warfare (EW) and RF sensing research
- Academic and industrial RF research

Description

The VORTARIAN 4R2T-10G is a coherent multi-channel SDR platform featuring four RF receive channels, two RF transmit channels and an FPGA-based processing subsystem. The system is optimized for applications requiring precise phase coherence, deterministic multi-channel timing and high dynamic range.

The combination of high-speed data converters, low-jitter clocking, dual 10 Gigabit Ethernet connectivity and support for external reference clocking makes the platform well suited for passive radar, direction finding, beamforming, distributed sensing and advanced wireless communications research.

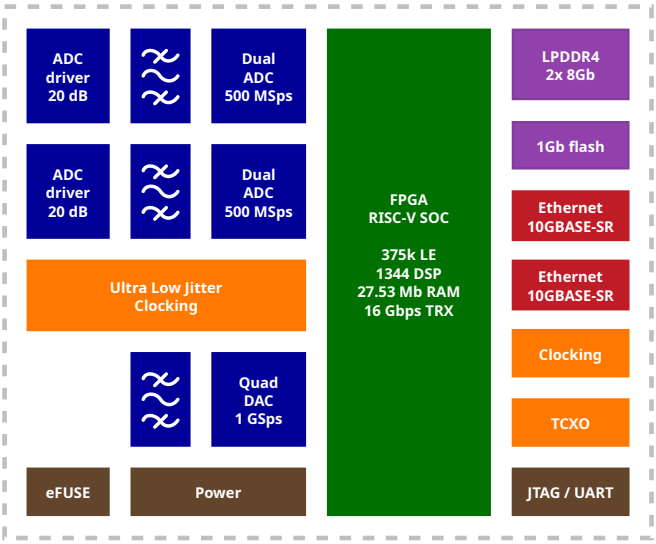

Figure 1: SDR functional block diagram

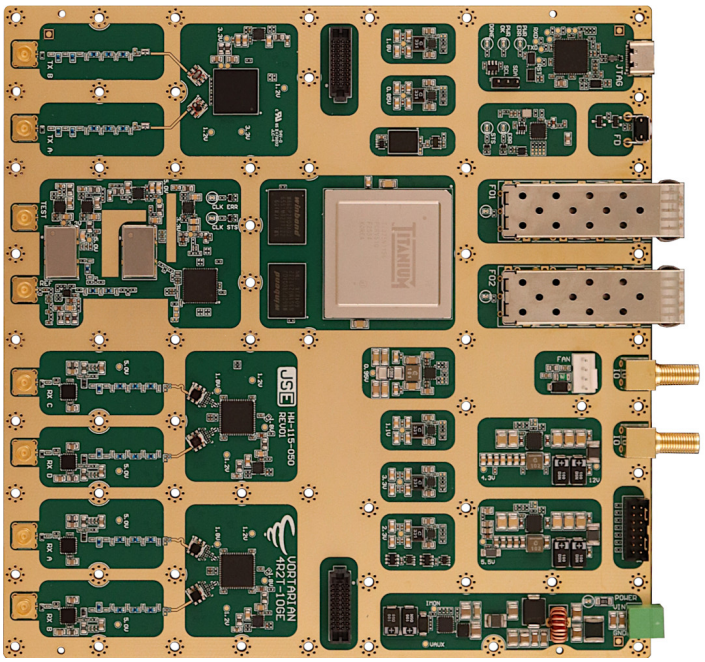

Figure 2: SDR platform board photo

Table 1: Hardware Overview

Platform Part Number	VORTARIAN 4R2T-10G (board + RF shielding enclosure)
Processing Board Part Number	HW-115-050 (available separately)
FPGA	Efinix Titanium Ti375N1156I3
CPU	Hardened Quad-Core 32-bit RISC-V processor
Memory	2× 8 Gb LPDDR4, dual independent LPDDR4 memory interfaces
ADC	Dual-channel, 500 MSPS, 16-bit
DAC	Quad-channel, 1000 MSPS, 16-bit

Table 2: Absolute Maximum Ratings

Parameter	*Maximum*	*Unit*
RX Input Power	-10	dBm
Reference Clock Input Power	+9	dBm
Supply Voltage	15	V
DC Voltage at RF Ports	7	V
Storage Temperature	-20 to +60	°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress limits only; functional operation at these conditions is not implied.

Table 3: DC and Power Characteristics

Input Supply Voltage	10 V to 14 V DC[1]
Power Consumption	19 W typical[2]

[1] Operation outside the specified supply-voltage range is not recommended.
[2] Power consumption depends on FPGA firmware and operating configuration.

Table 4: Clocking and Synchronization

Reference Clock Frequency	100 MHz ± 10 ppm
Reference Clock Input Level	recommended signal level ≈ +6 dBm ± 3 dB[1]
Reference Clock Port Impedance	50 Ω
Reference Clock Input Coupling	AC-coupled
Internal Reference	ultra-low-phase-noise 100 MHz ± 20 ppm reference clock
External Reference	external ultra-low-phase-noise 100 MHz OCXO reference clock supported
Clock Generation	ultra-low-jitter coherent clock generation and distribution
Reference Distribution	external reference clock distribution, configurable as input or output
Multi-Board Synchronization	hardware support for future coherent multi-board synchronization
Coherent Operation	multi-channel phase-coherent acquisition and RF front-end calibration support[2]

[1] Operation with a reference signal outside the specified limits may degrade phase-noise performance.
[2] Final phase stability and calibration performance depend on the complete RF front-end, antenna system, and operating conditions.

Table 5: RF Characteristics

Parameter	*Conditions*	*Value*	*Unit*
Interface			
RX Channels	coherent receive channels	4	–
TX Channels	transmit channels	2	–
Port Impedance	RX and TX ports	50	Ω
Port Coupling	RX and TX ports	AC-coupled	–
RX Characteristics			
Analog Input Frequency Range	direct RF / IF sampling	20 to 1400	MHz
Standard RX Passband	standard RF front-end assembly[1]	250 to 500	MHz
Passband Center Frequency	standard RF front-end assembly	375	MHz
Gain	standard 2nd-Nyquist-zone configuration	18.93	dB
Gain Flatness	250 to 500 MHz	0.55	dB p-p
Input Return Loss	typical measured	17.4	dB
SFDR	$f_{RF} = 404-406$ MHz, $P_{RF} = -12$ dBm	> 91.4	dBc
Maximum Input Power	normal operating limit	≈ -10	dBm
Amplifier Gain	typical	20	dB
Amplifier OIP3	$f_{RF} = 240$ MHz[2]	46.2	dBm
Filtering	standard RF front-end	band-pass filtering	
Input Protection	bidirectional ESD protection	±20 kV IEC 61000-4-2, $C_{IO} \approx 0.1$ pF	
TX Characteristics			
Maximum Output Power	standard RF front-end	≈ -8	dBm
Filtering	standard RF front-end	band-pass filtering	

[1] The standard RF front-end assembly is optimized for operation in the second Nyquist zone (250 MHz to 500 MHz). The analog RF input supports direct RF / IF sampling from 20 MHz to 1.4 GHz. Alternative RF front-end configurations can be provided for application-specific frequency ranges and responses.

[2] The OIP3 value refers to amplifier specification and does not represent the measured OIP3 of the complete RX signal chain.

Table 6: Digital Interfaces and Data Streaming

Ethernet Interface ETH0	10GBASE-SR, SFP+ cage
Ethernet Interface ETH1	10GBASE-SR, SFP+ cage
Ethernet MTU	jumbo frames supported, MTU up to 9000 bytes
Data Streaming	continuous I/Q streaming after digital downconversion
Streaming Configuration Example	4 channels at 125 MSPS, 16-bit I/Q, aggregate data rate 2×8 Gbps
Interface Throughput	sustained near-line-rate operation on dual 10GbE interfaces
Software Interface	GNU Radio compatible

Table 7: Mechanical Characteristics

PCB Construction	14-layer, controlled-impedance, high-Tg laminate (Tg 170 °C)
Board Dimensions	177 mm × 177 mm
Enclosure Dimensions	180 mm × 180 mm

RF Mezzanine Front-Ends

The VORTARIAN 4R2T-10G supports application-specific RF mezzanine front-ends for extending the operating frequency range beyond the native direct RF / IF sampling range of the processing board. The mezzanine architecture provides RF frequency conversion and signal conditioning while preserving the coherent multi-channel architecture of the base SDR platform.

A reference implementation has been developed for operation in the 2.4 GHz ISM band. The front-end provides four coherent RF receive paths, two RF transmit paths and more than 100 MHz of instantaneous RF bandwidth. One transmit path is dedicated to integrated multi-channel phase calibration support.

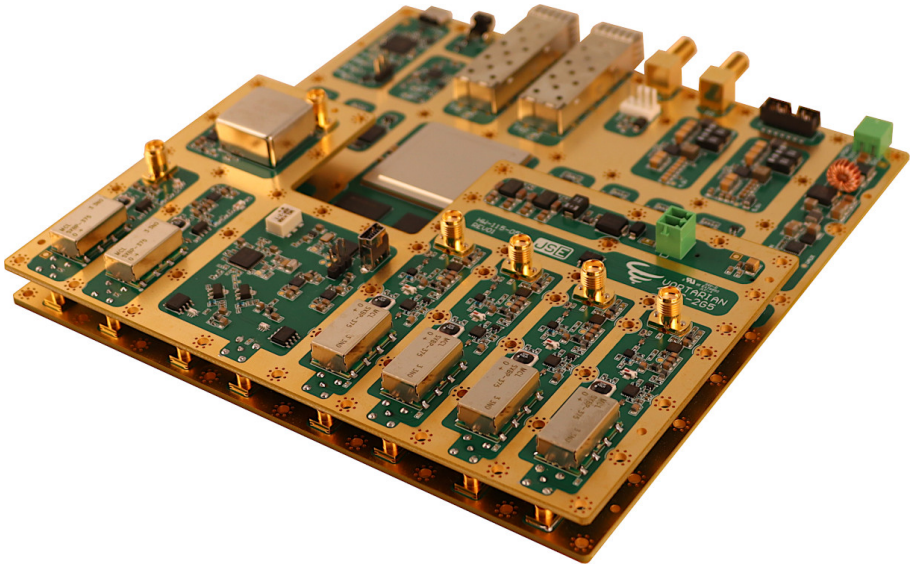

Figure 3: VORTARIAN 4R2T-10G with 2.4 GHz ISM-band RF mezzanine front-end

Table 8: RF Mezzanine Front-End Overview

Architecture	application-specific RF frequency-conversion mezzanine
Reference Implementation	2.4 GHz ISM-band RF front-end
Instantaneous RF Bandwidth	$>$ 100 MHz
RX Channels	4× coherent RF receive paths
TX Channels	2× RF transmit paths, integrated multi-channel phase calibration support.
Phase Calibration	integrated multi-channel phase calibration support
Frequency Reference	on-board 100 MHz low-phase-noise OCXO
Reference Stability	±50 ppb
RF Interface	50 Ω RF interfaces
RX Gain Modes	selectable low-gain and high-gain receive modes
RX Noise Figure	2.7 dB typical, simulated in high-gain configuration
RX Input Sensitivity	approximately −111 dBm at 1 MHz bandwidth and 0 dB SNR, simulated
Customization	RF mezzanine front-ends can be adapted for application-specific frequency bands, filtering, gain and signal levels[1]

[1] RF performance, frequency coverage and electrical characteristics depend on the specific mezzanine configuration.

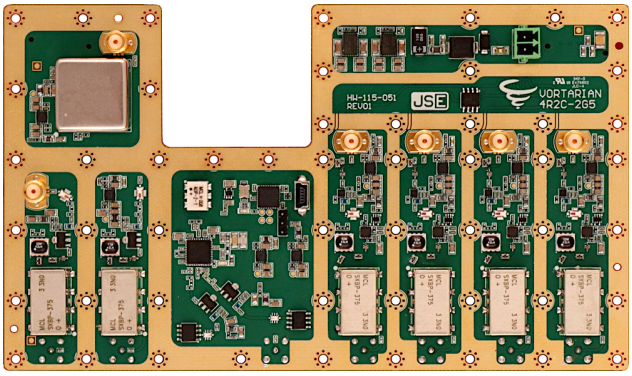

Figure 4: Reference 2.4 GHz RF mezzanine front-end, top view

Modular RF Architecture

The mezzanine converts the application RF band into the native operating range of the VORTARIAN 4R2T-10G while retaining the platform clocking, synchronization, FPGA processing and high-speed data-streaming infrastructure.

The on-board low-phase-noise OCXO provides a stable common frequency reference for the RF conversion circuitry. Together with the integrated phase-calibration path, this architecture is intended for coherent multi-channel applications such as direction finding, beamforming, passive radar and distributed RF sensing.

Alternative mezzanine implementations can target other microwave and mmWave frequency bands without modification of the main processing board.

Clocking Performance

Table 9: Typical ADC Sampling Clock Integrated Jitter at 500 MHz ADC Sampling Rate

Integration Bandwidth	*Integrated Jitter [fs][1]*
1 kHz to 10 MHz	30.4
1 kHz to 100 MHz	50.3
1 Hz to 100 MHz	607

[1] Typical measured values. Actual performance may vary depending on component tolerances, operating conditions and reference clock source.
[2] Phase-noise and integrated-jitter characterization performed using a Rohde & Schwarz FSWP phase-noise analyzer.

Table 10: Typical ADC Sampling Clock Phase Noise at 500 MHz ADC Sampling Rate

Offset Frequency	*Phase Noise [dBc/Hz]*
1 Hz	-54.54
10 Hz	-78.96
100 Hz	-107.73
1 kHz	-112.02
10 kHz	-138.35
100 kHz	-155.36
1 MHz	-159.27
10 MHz	-160.00
100 MHz	-160.54
300 MHz	-161.23

[1] Typical measured values. Actual performance may vary depending on component tolerances, operating conditions and reference clock source.
[2] Phase-noise and integrated-jitter characterization performed using a Rohde & Schwarz FSWP phase-noise analyzer.

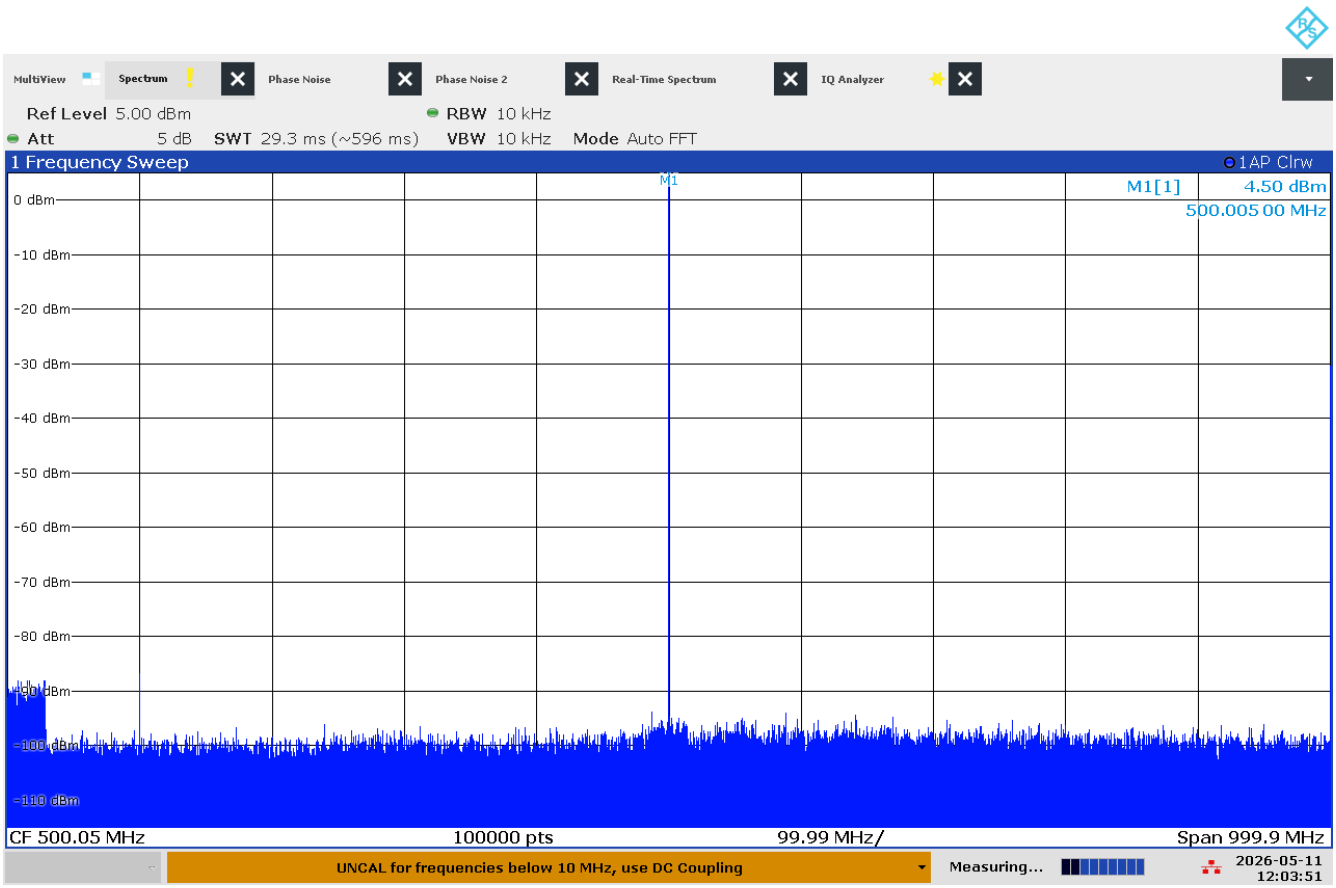

Figure 5: ADC Sampling Clock Spectral Purity, Rohde & Schwarz FSW analyzer

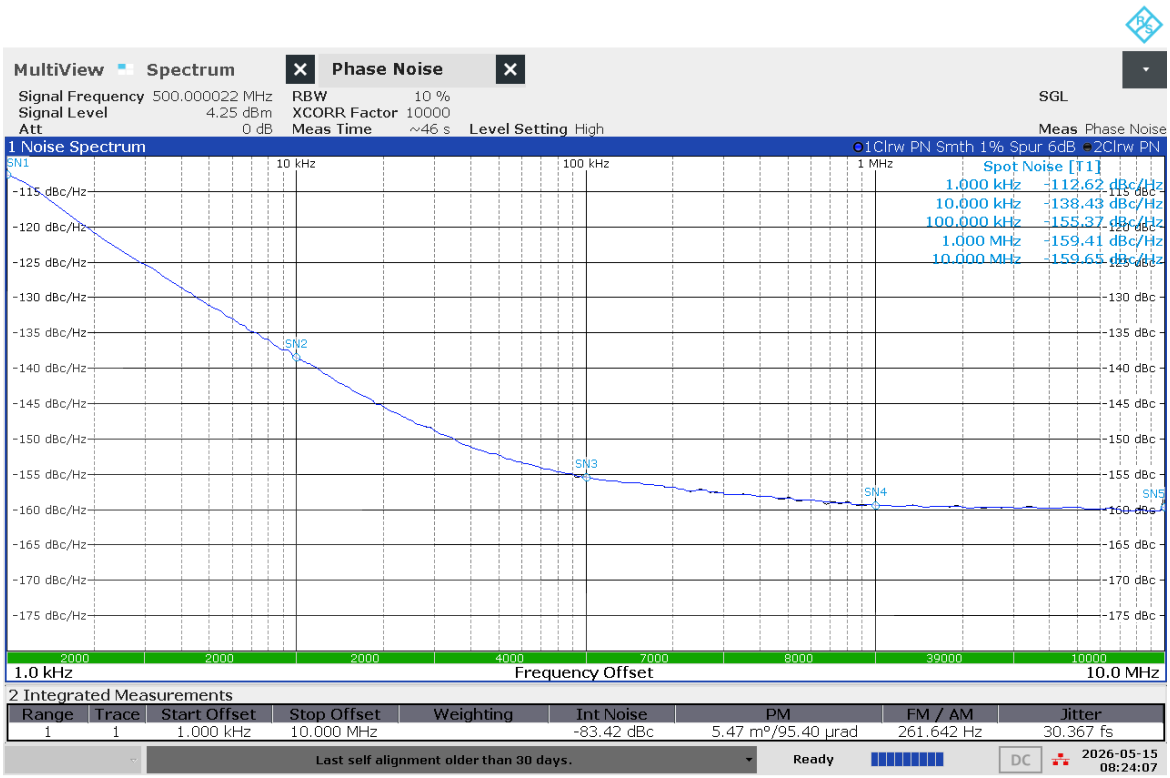

Figure 6: ADC Sampling Clock Characterization (500 MHz), 1 kHz to 10 MHz Integration Bandwidth, Rohde & Schwarz FSWP analyzer

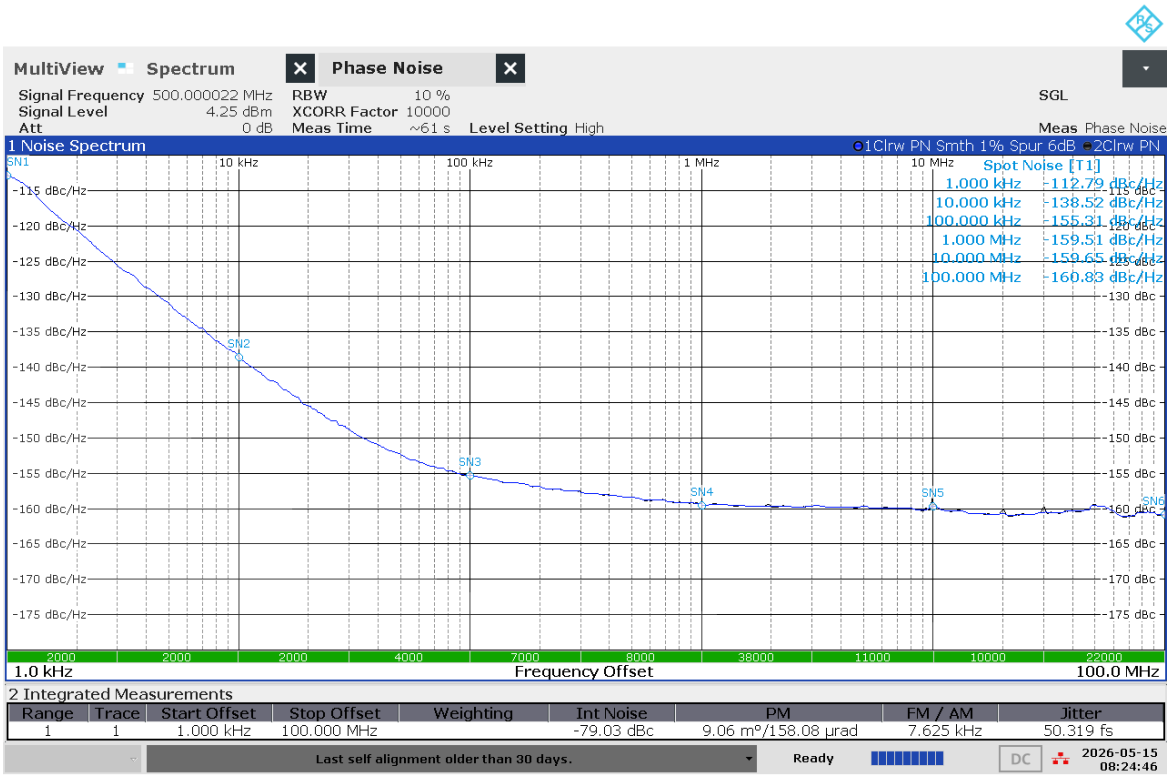

Figure 7: ADC Sampling Clock Characterization (500 MHz), 1 kHz to 100 MHz Integration Bandwidth, Rohde & Schwarz FSWP analyzer

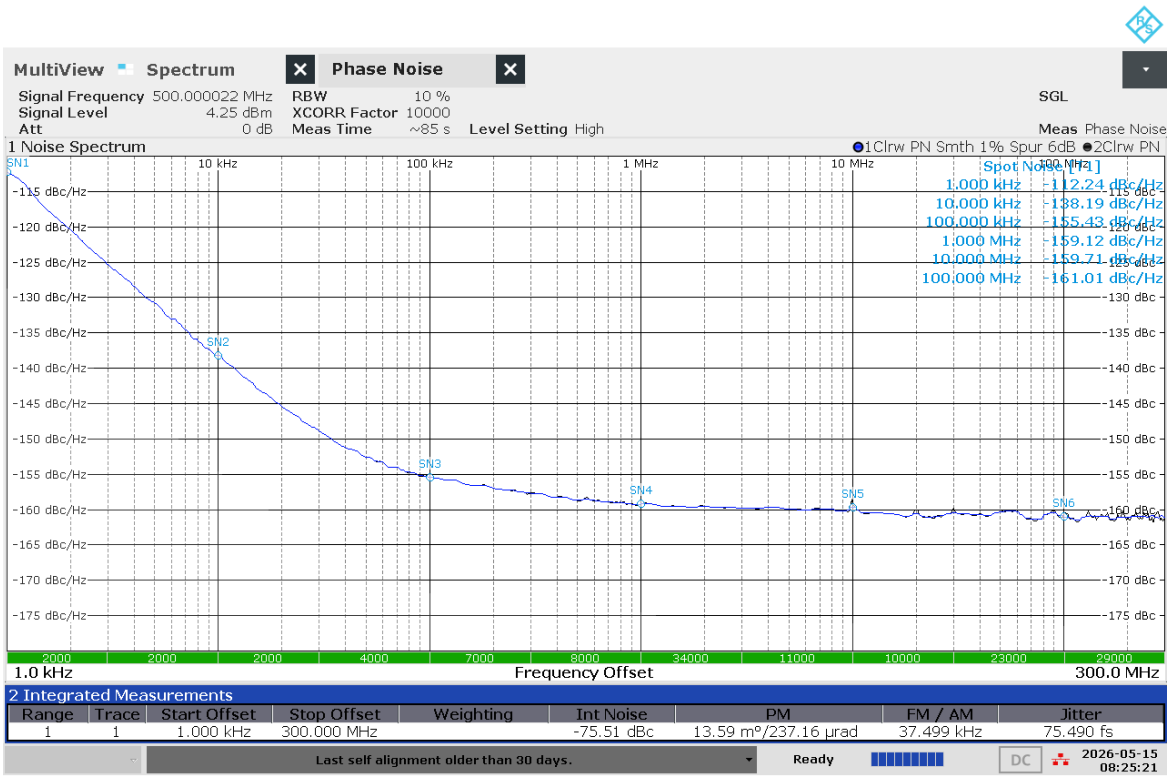

Figure 8: ADC Sampling Clock Characterization (500 MHz), 1 kHz to 300 MHz Integration Bandwidth, Rohde & Schwarz FSWP analyzer

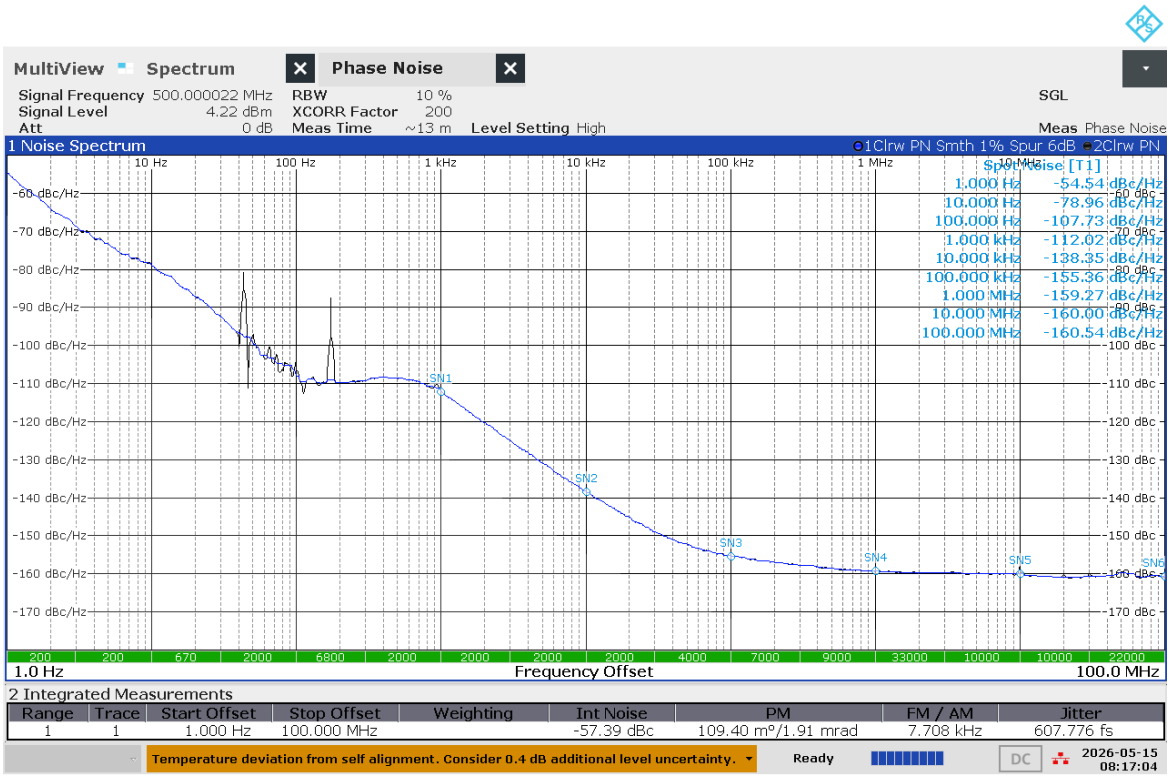

Figure 9: ADC Sampling Clock Characterization (500 MHz), 1 Hz to 100 MHz Integration Bandwidth, Rohde & Schwarz FSWP analyzer

ADC Dynamic Performance

The plots below illustrate the calculated complex power spectra derived from 256 k I/Q samples with a 16-bit resolution. The input test tone (fundamental frequency) is explicitly marked in the graphs with a red circle ○.

Since the input to the Digital Downconverter (DDC) is a real-valued signal while the output is complex, the resulting spectrum inherently contains the image component corresponding to the negative fundamental frequency ($-f_{IN}$). Due to the frequency shift around the carrier frequency f_C, this image response appears at the folded frequency position and is designated with a red cross ×.

Any additional spurious components exceeding the $-95\ dBFS$ threshold are automatically identified and highlighted with a red square □, provided they exist within the displayed spectrum.

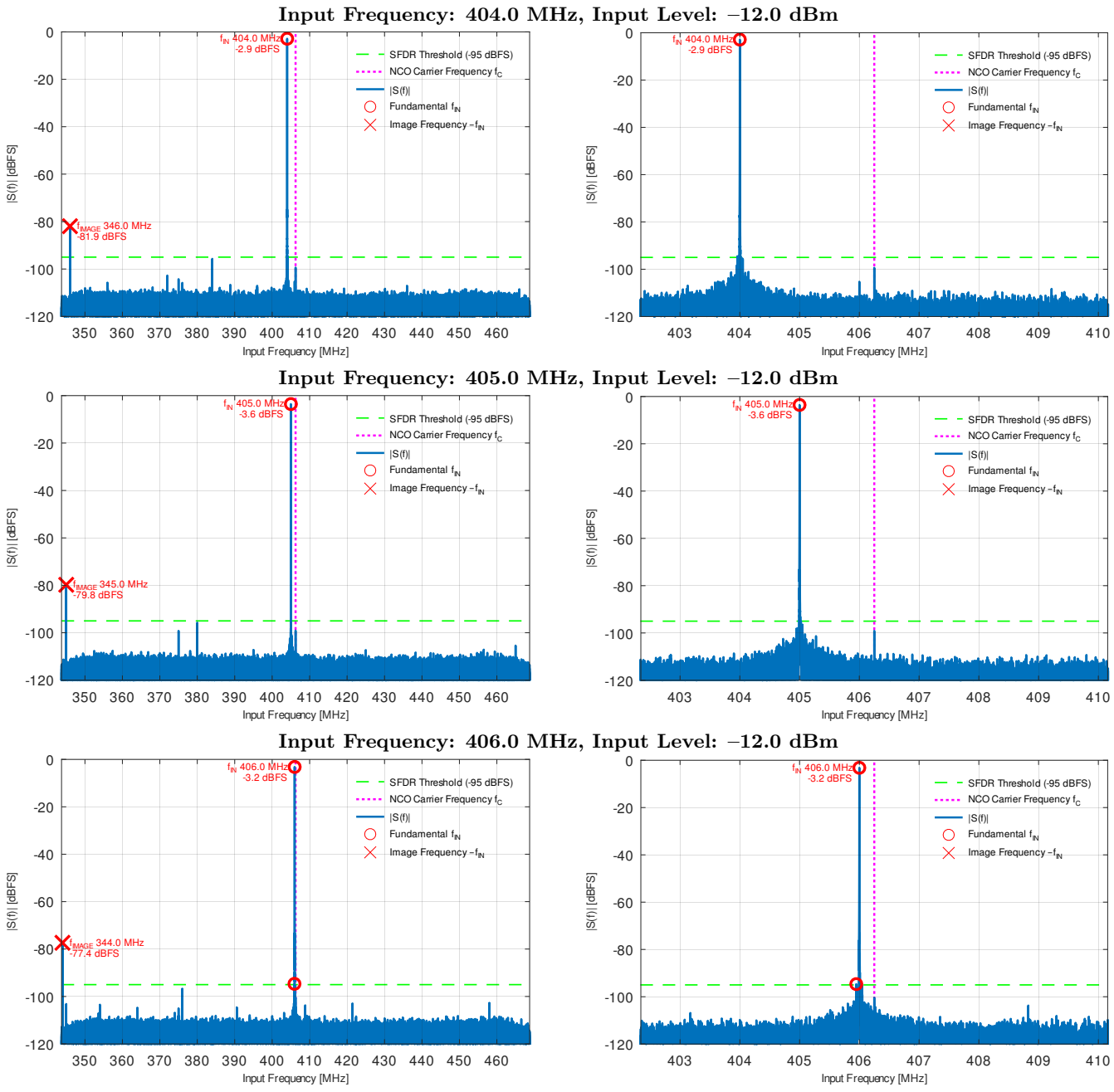

Figure 10: Typical ADC Dynamic Performance, 500 MSPS Sampling Rate, 256k Complex FFT

DAC Output Phase Noise

The DAC output phase-noise performance was characterized using a Rohde & Schwarz FSWP phase-noise analyzer. The measurement was performed with a 406.25 MHz output tone generated by the on-board DAC operating at a 1 GSPS sampling rate.

Integrated RMS jitter (10 Hz to 100 MHz): 172 fs.

Table 11: Typical DAC Output Phase Noise

Offset Frequency	*Phase Noise [dBc/Hz]*
10 Hz	-81.8
100 Hz	-108.0
1 kHz	-114.2
10 kHz	-132.9
100 kHz	-141.0
1 MHz	-145.8
10 MHz	-151.8
100 MHz	-155.5

[1] Typical measured values. Actual performance may vary depending on component tolerances, operating conditions and reference clock source.
[2] Phase-noise and integrated-jitter characterization performed using a Rohde & Schwarz FSWP analyzer.

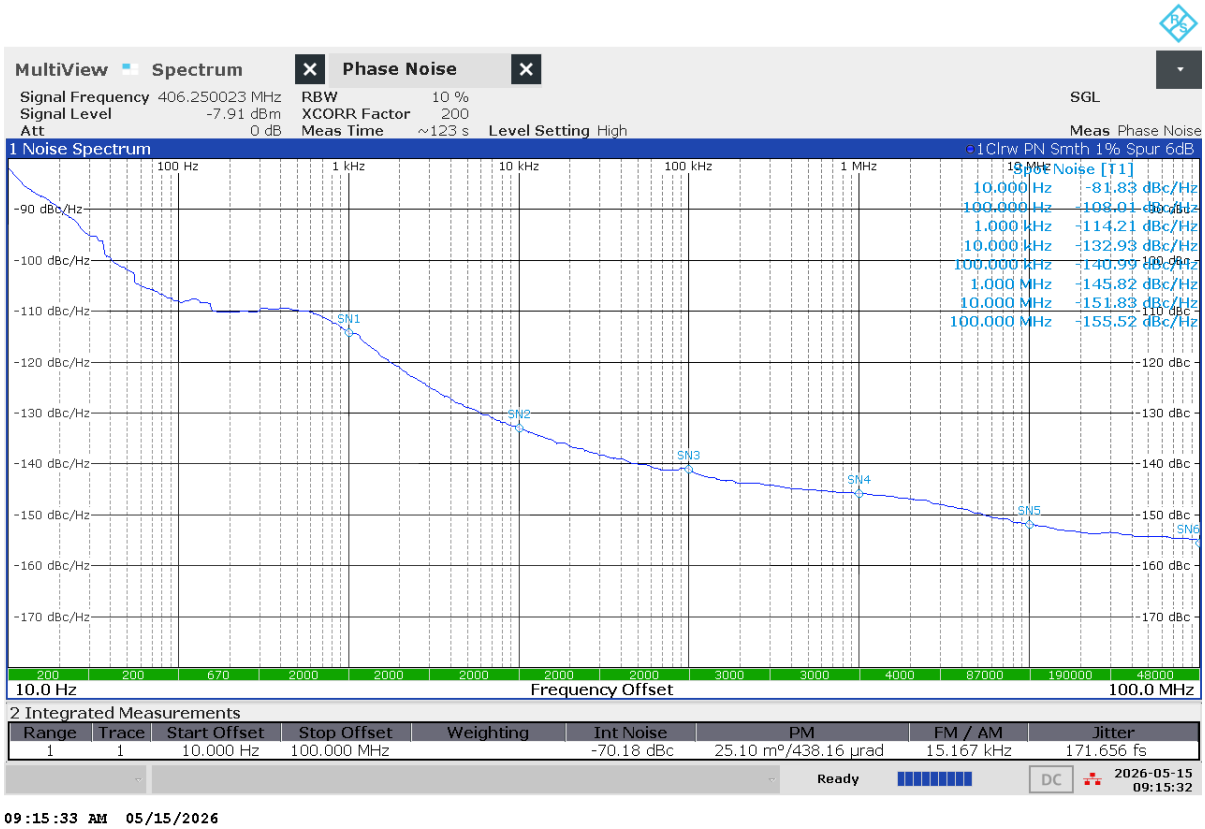

Figure 11: Typical DAC output phase noise, 406.25 MHz output frequency

Revision History

Revision	*Date*	*Description*
1.00	June 05, 2026	Initial release
1.01	June 10, 2026	Added clocking characterization
1.02	June 19, 2026	Added ADC dynamic performance
1.03	July 4, 2026	Platform rebranding
1.04	August 27, 2026	Added mezzanine up/down-converter support
1.05	September 6, 2026	Created a public version of the datasheet

Customization

This product is available for customization to meet specific application requirements. JSE s.r.o. offers custom development services in RF, microwave and FPGA design. Customization and development services are provided under the applicable JSE s.r.o. Business Terms and Conditions. For inquiries, contact sales@jse.dev.

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